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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,365	09/04/2003	Michael Norman Day	AUS920030531US1	8448
45327	7590	10/21/2005	EXAMINER	
IBM CORPORATION (CS) C/O CARR LLP 670 FOUNDERS SQUARE 900 JACKSON STREET DALLAS, TX 75202			DOAN, DUC T	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/655,365

Applicant(s)

DAY ET AL.

Examiner

Duc T. Doan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10/3/05</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Status of Claims***

Claims 1-21 are in the application.

Claims 1-21 are rejected.

### ***Claim Objections***

Claim 13 is objected to because of the following informalities:

As per claim 13, the recitation “the second cache” lacks antecedent basis. Furthermore, in light of the specification page 20 lines 21-32, Examiner interprets the claim as following: “..step of retrieving the data associated with an address from the cache if there is a **miss** in the cache”

Appropriate correction is required.

### ***Double Patenting***

Claim 1 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending application 10/655367, and inview of Arimilli’s et al (US 6425058). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Copending Application, 10/655367; Claim 1	Instant Application, 10/655365; Claim 1
A software controlled data replacement system	A software controlled data replacement system

<p>for a cache, the system employing a class identifier and a tag replacement control indicia, comprising:</p> <p>'797 does not describe the claim's aspect of memory region. However, Arimilli's column 9 lines 3-44 describe virtual cache's memory area is indexed and identified in a congruence class. It would have been It would have been obvious to one of ordinary skill in the art at the time of invention to include memory region and classes as suggested by Arimilli in '795 system to create virtual caches and selective tuning for different types of data and information thereby extracting maximum performance from a cache architecture (Arimilli's column 9 lines 7-12)</p>	<p>for a cache, the system employing a <b>memory region</b> and <b>associated</b> class identifier and a tag replacement control indicia, comprising:</p>
<p>a replacement management table, employable to read the class identifier to create the tag replacement control indicia; and</p>	<p>a replacement management table, employable to read the class identifier to create the tag replacement control indicia; and</p>
<p>the cache, comprising a plurality of sets, employable to disable a replacement of at least</p>	<p>the cache, comprising a plurality of sets, employable to disable a replacement of at least</p>

one of the plurality of sets as a function of the tag replacement control indicia.	one of the plurality of sets as a function of the tag replacement control indicia.
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***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-6,8-21 rejected under 35 U.S.C. 102 (e) as being anticipated by Arimilli et al (US 6425058).

As for claim 1, Arimilli describes a software controlled data replacement system for a cache, the system employing a memory region and associated class identifier and a tag replacement control indicia (Arimilli's column 7 lines 5-55), comprising: a replacement

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management table (Arimilli's Fig 5, Fig 7; column 6 lines 1-27 describes virtual caches management whereas each virtual cache element, "a row", is further partitioned into multiple types and set associative), employable to read the class identifier (virtual caches ID) to create the tag replacement control indicia (Fig 7: #130 a virtual cache's ITF setting to information type field) (Arimilli's Fig 5, 7; column 5 line 65 to column 6 line 27 describes using virtual cache value in control register 132 to select a virtual cache's ITF setting; the ITF setting determines cache partitioning and set associative for replacement of data in a virtual cache; Arimilli's column 6 lines 53-66 further describes using virtual caches' performance to determine the replacing of virtual caches), wherein the class identifier is created by software (Arimilli's column 8 lines 49-52); and the cache, comprising a plurality of sets, employable to disable a replacement of at least one of the plurality of sets as a function of the tag replacement control indicia (Arimilli's Fig 5, column 6 lines 5-27 describes the virtual caches' sets can be managed to be overlapped or disjointed).

As for claims 2-6 Arimilli describes wherein the memory region and associated class identifier creation software further comprises compiler or operating system software (claim 2; column 6 lines 45-53); wherein a set of the cache is replaced based upon a least recently used function (claim 3; column 9 lines 30-45); wherein the replacement management table uses software (claim 4; column 6 lines 45-53); wherein class identifier creation software is employable to classify an address range as a default address range (claim 5; column 6 lines 27-30; predetermined by hardware); wherein the cache comprises a translation lookaside buffer (claim 6; column 6 lines 50-66);

As for claim 8, the claim recites a method of determining information replacement in a cache, comprising: creating a class identifier by class identifier creation software; reading the class identifier; creating a tag replacement control indicia as a function of the class identifier through employment of a replacement management table; and configuring replacement eligibility of a set in a cache as a function of the associated tag replacement control indicia. The claim rejected base on the same rationale as in the rejection of claim 1.

Claim 9 rejected based on the same rationale as in the rejection of claim 2.

Claims 10,14,19 rejected based on the same rationale as in the rejection of claim 3.

Claim 11 rejected based on the same rationale as in the rejection of claim 5. Arimilli describes the information can be a combination of partially software programmable and partly predetermined by hardware (Arimilli's column 6 lines 27-50).

As for claims 12-13, the claim recites further comprising discarding the tag replacement control indicia if there is a hit on the cache (claim 12); the step of retrieving the data associated with an address from the second cache if there is a hit in the second cache (claim 13). It is obvious that if the result of TLB is a hit on the cache, the corresponding "hit translation" entry in the TLB is kept; and the data will be retrieved from memory in case of a miss. Arimilli describes of monitoring the hit/miss of virtual caches to determine of replacing virtual caches (Arimilli's column 8 lines 53-67).

As for claim 15, the claim recites employing an address range to associate with the class identifier. Arimilli describes the virtual caches associating with different disjointed sets of addresses (Arimilli's Fig 5; column 6 lines 1-28).

As for claim 16 the claim recites employing an algorithm bit to select an algorithm for the replacement of the eligible set. Arimilli describes that different allocation/replacement policies are implemented with virtual caches using the contents of information type fields (Arimilli's column 9 lines 5-45). Thus Arimilli's clearly suggests using bits in the information type field to determine the replacement policies.

Claim 17 rejected based on the same rationale as in the rejection of claim 11.

Claims 18,21 rejected based on the same rationale as in the rejection of claim 1.

Claim 20 rejected based on the same rationale as in the rejection of claim 5.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Arimill et al (US 6425058) as applied to claim 4, and further in view of Chauvel et al (US 6826652).

As for claim 7, the claim recites wherein class identifier generation software further comprises a direct memory access command. Arimilli does not describe the claim's detail of direct memory access. However Chauvel describes a cache capable to be configured to operate in



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normal or ram-set modes whereas in ram-set mode data are filled through DMA (Chauvel's column 5 line 45 to column 6 line 10). It would have been obvious to one of ordinary skill in the art at the time of invention to include ram-set mode as suggested by Chauvel in Arimilli's system to preventing the cache miss for critical codes in cache (Chauvel's column 5 lines 55-60).

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Loen (US 6430667).

Arimilli et al (US 6430656).

Yoshioka et al (US 5796978).

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Kevin L. Ellis**  
**Primary Examiner**

*Kevin L. Ellis*